Grigoris D. Dimitroulakos

3rd grade Academic Laboratory Instructor

Informatics and Telecommunications Department

University of Peloponnese

Curriculum Vitae

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1.1 Personal Information

Name/Surname	Grigoris D. Dimitroulakos
Birth Date	26/03/1976
Marital Status	Married
Email	dhmhgre@uop.gr
Personal Webpage	http://users.uop.gr/~dhmhgre/

1.2 Education

1994-1999	Bachelor in Physics, Physics Department, University of Patras
1999-2001	Master in Electronics, Physics Department, University of Patras
2001-2007	Phd in Computer Science, Electrical and Computer Engineering Department, University of Patras

1.3 Professional Experience

2008-σήμερα	Academic Laboratory Instructor in Informatics and Telecommunications Department of University of Peloponnese since 2008
01/2010- 12/2012	Participation in the 7th Framework European Project ENOSYS (ICT-2009.3.4), "intEgrated modelliNg and synthesis tOol flow for embedded SYStems design"
09/2011-08/2014	Participation in the 7th Framework European Project ALMA (ICT-2011. 287733), "Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb"
2001-2004	Participation in the European Project EASY (IST-2000-30093), "Energy-Aware SYstem-On-Chip design of the HiperLan/2 standard"
06/2002-11/2002	6-month employee in IMEC (Interuniversity MicroElectronics Center, www.imec.be)

1.4 Research Interests & Skills

Programming Languages and Software Packages	C, C++, C#, .NET, Java, Scilab, MATLAB, BNF notation, UML,.NET, VHDL, Win32, WPF,
Software Tool Development	α) Design Automation Tool for source transformations (MEMSCOPT- 60000 code lines) β) Design Automation tool for translation of Scilab to C language (SAFE- 75000 lines of code) γ) Cache Memory Simulation Tool (XMSIM- 3000 lines) δ) Compiler Front-End generation tool (3000 lines) ε) Compiler Back-End targeting Coarse Grain Reconfigurable Architectures (25000 lines)
Research Interests	Compilers, Programming Languages, Compiler Design, Object Oriented Development, Object Orient Design Patterns, High Level Synthesis, .NET
Software Development Tools	flex, bison, ANTLR, Purify Plus, MATLAB, Scilab, Microsoft Visual Studio, Modelsim, MSBuild

1.5 Teaching Experience

2003-2006	Teaching assistant in the Master course «Software for Embedded Systems Design" (Electrical and Computer Engineering Dep, University of Patras)
2002-2004	Laboratory Teaching assistant for the undergraduate course «Design of Integrated Circuits with VLSI techniques». (Electrical and Computer Engineering Dep, University of Patras)
2004-2005	Laboratory Teaching assistant for the undergraduate course «Logic Design». (Electrical and Computer Engineering Dep, University of Patras)
2008-2016	Laboratory Teacher and organizer for the following undergraduate courses : Computer Architecture I, Compilers I, Computer Architecture II, Compilers II (Informatics and Telecommunication Dep, University of Peloponnese)
2011-2012	Teaching in the postgraduate course «Embedded Systems» (Informatics and Telecommunication Dep, University of Peloponnese)
2012-2014	Teaching in the postgraduate courses «Embedded Systems Software», και «Embedded systems compilation tools", (Informatics and Telecommunication Dep, University of Peloponnese)
2011-2012, 2013-2016	Teaching the undergraduate course Compilers I
2011-2012, 2013-2014	Teaching the undergraduate course Computer Architecture I
2012-2013	Teaching the undergraduate course Compilers II

1.6 Seminars

2001, 2003	DTSE (Data Transfer and Storage Exploration) Seminar (IMEC Interuniversity Microelectronics Center)
2002, 2003	System Design Metaflow Seminar (IMEC Interuniversity Microelectronics Center)

1.7 Foreign Languages

English	2005 Cambridge 1st Certificate (Lower) 2006 Michigan Proficiency

1.8 Publications

Journals (16)

1. Chris Karanikolas,Grigoris Dimitroulakos,Konstantinos Masselos: Early Evaluation of Implementation Alternatives of Composite Data Structures Towards Maintainability. To Appear in ACM Transactions on Software Engineering and Methodology (TOSEM)
2. Ioannis Latifis, Karthick Parashar, Grigoris Dimitroulakos, Hans Cappelle, Christakis Lezos, Konstantinos Masselos, Francky Catthoor: A MATLAB Vectorizing Compiler Targeting Application-Specific Instruction Set

Processors. ACM Trans. Design Autom. Electr. Syst. 22(2): 32:1-32:28 (2017)
3. Theodoros Lioris, Grigoris Dimitroulakos, Konstantinos Masselos: An early memory hierarchy evaluation simulator for multimedia applications. Microprocessors and Microsystems - Embedded Hardware Design 38(1): 31-41 (2014)
4. Timo Stripf, Oliver Oey, Thomas Bruckschlögl, Jürgen Becker, Gerard K. Rauwerda, Kim Sunesen, George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Steven Derrien, Olivier Sentieys, Nikolaos Kavvadias, Grigoris Dimitroulakos, Kostas Masselos, Dimitrios Kritharidis, Nikolaos Mitas, Thomas Perschke: Compiling Scilab to high performance embedded multicore systems. Microprocessors and Microsystems - Embedded Hardware Design 37(8-C): 1033-1049 (2013)
5. Grigoris Dimitroulakos, Stavros Georgiopoulos, Michalis D. Galanis and Costas E. Goutis, "Resource aware mapping on coarse grained reconfigurable Arrays Microprocessors and Microsystems - Embedded Hardware Design}, vol. 33, no. 2, 2009, pp. 91-105
6. Grigoris Dimitroulakos, Nikos Kostaras, Michalis D. Galanis, and Costas E. Goutis, "Compiler assisted architectural exploration framework for coarse grained reconfigurable arrays", The Journal of Supercomputing, vol. 48, no.2, 2009, pp. 115-151
7. Michalis D. Galanis, Gregory Dimitroulakos and Costas E. Goutis, "Performance and Energy Consumption Improvements in Microprocessor Systems Utilizing a Coprocessor Data-Path", Journal of Signal Processing Systems, vol. 50,no. 2, 2008, pp. 179-200
8. G. Dimitroulakos, N.D Zervas, N. Sklavos, and C.E. Goutis, "Design techniques and implementation of Low power high-throughput Discrete Wavelet transform filters for JPEG 2000 Standard", to appear in International Journal of Signal Processing, vol.4 no.1 2008, World Enformatica
9. Michalis D. Galanis, Gregory Dimitroulakos, Spyros Tragoudas and Costas E. Goutis}, "Speedups in embedded systems with a high-performance coprocessor datapath", ACM Trans. Design Autom. Electr. Syst., vol. 12, no. 3, 2007
10. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis, "Speedups and Energy Reductions From Mapping DSP Applications on an Embedded Reconfigurable System" IEEE Trans. VLSI Syst. vol. 15 no.12, pp. 1362-1366 2007
11. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis, "Exploring the speedups of embedded microprocessor systems utilizing a high-performance coprocessor data-path", The Journal of Supercomputing vol. 39 no.3 pp. 251-271 2007
12. Grigoris Dimitroulakos, Michalis D. Galanis, Costas E. Goutis, "Design space exploration of an optimized compiler approach for a generic reconfigurable array architecture" The Journal of Supercomputing vol. 40, no.2 pp. 127-157, 2007
13. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis, "Performance Improvements from Partitioning Applications to FPGA

Hardware in Embedded SoCs", The Journal of Supercomputing vol. 35, no.2, pp. 185-199, 2006

14. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis, "Partitioning Methodology for Heterogeneous Reconfigurable Functional Units", The Journal of Supercomputing vol. 38, no. 1, pp. 17-34, 2006
15. Grigoris Dimitroulakos, Michalis D. Galanis, Athanasios Milidonis, Constantinos E. Goutis, "A high-throughput, memory efficient architecture for computing the tile-based 2D discrete wavelet transform for the JPEG2000", Integration the VLSI Journal vol. 39, no.1, pp. 1-11 2005
16. A. Milidonis, G. Dimitroulakos, M. D. Galanis, A. P. Kakarountas, G. Theodoridis, C. E. Goutis, and F. Catthoor, "A Framework for Data Partitioning for C++ Data-Intensive Applications", Design Automation for Embedded Systems (DAES), Springer, vol. 9, no. 2, pp. 101-121, 2004

Conferences (38)

1. Christakis Lezos, Grigoris Dimitroulakos, Ioannis Latifis, Konstantinos Masselos, “MAFE: An Environment for MATLAB-to-C Compilation Supporting Static and Dynamic Memory Allocation and Multi-Level User Interactive Code Optimization”, in Proceedings of the 2016 International Symposium on Code Generation and Optimization (CGO), Barcelona, Spain, March 12-18, 2016, [Poster session].
2. Christakis Lezos, Ioannis Latifis, Grigoris Dimitroulakos, Konstantinos Masselos, “Compiler-Directed Data Locality Optimization in MATLAB” in Proceedings of the 19th International Workshop on Software and Compilers for Embedded Systems (SCOPES), Sankt Goar, Germany, May 23-25th, 2016.
3. Christakis Lezos, Grigoris Dimitroulakos, Ioannis Latifis, Konstantinos Masselos, “Automatic Generation of Code Analysis Tools: The CastQL Approach”, in Proceedings of the 1st International Workshop on Real World Domain Specific Languages (RWDSL), held in conjunction with the 2016 International Symposium on Code Generation and Optimization (CGO), Barcelona, Spain, March 12-18, 2016.
4. Ioannis Latifis, Karthick Parashar, Grigoris Dimitroulakos, Hans Cappelle, Christakis Lezos, Konstantinos Masselos and Francky Catthoor, “Matlab-to-C compilation targeting Application Specific Instruction Set Processors”, in Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany, March 14-18, 2016.
5. Christakis Lezos, Grigoris Dimitroulakos, Angeliki Freskou, Konstantinos Masselos: Dynamic source code analysis for memory hierarchy optimization in multimedia applications. DASIP 2013: 343-344
6. Grigoris Dimitroulakos, Theodoros Lioris, Christakis Lezos, Konstantinos Masselos: XMSIM: A tool for early memory hierarchy evaluation. DASIP 2012: 1-2
7. Grigoris Dimitroulakos, Christakis Lezos, Konstantinos Masselos: MEMSCOPT: A source-to-source compiler for dynamic code analysis and loop transformations. DASIP 2012: 1-2
8. Timo Stripf, Oliver Oey, Thomas Bruckschlögl, Ralf König, Michael Hübner, Jürgen Becker, Gerard K. Rauwerda, Kim Sunesen, Nikolaos Kavvadias, Grigoris Dimitroulakos, Kostas Masselos, Dimitrios Kritharidis, Nikolaos Mitas, George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Steven

Derrien, Daniel Menard, Olivier Sentieys, Diana Göhringer, Thomas Perschke: A flexible approach for compiling scilab to reconfigurable multi-core embedded systems. ReCoSoC 2012: 1-8
9. George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Christos Valouxis, Christos Gogos, Nikolaos Kavvadias, Grigoris Dimitroulakos, Kostas Masselos, Diana Göhringer, Steven Derrien, Daniel Menard, Olivier Sentieys, Michael Hübner, Timo Stripf, Oliver Oey, Jürgen Becker, Gerard K. Rauwerda, Kim Sunesen, Dimitrios Kritharidis, Nikolaos Mitas: From Scilab to multicore embedded systems: Algorithms and methodologies. ICSAMOS 2012: 268-275
10. Theodoros Lioris, Grigoris Dimitroulakos, Kostas Masselos: XMSIM: EXtensible Memory SIMulator for Early Memory Hierarchy Evaluation. ISVLSI 2010: 375-380
11. Grigoris Dimitroulakos, Stavros Georgiopoulos, Nikos Kostaras and Costas Goutis, "Embedding High Performance Multipliers in Coarse Grain Reconfigurable Array Architectures",16 IFIP/IEEE International Conference VLSI-SOC, 2008
12. Georgiopoulos, S., G. Dimitroulakos, G. and Goutis, C.E., " Integrating high speed multipliers in Coarse Grain Reconfigurable Arrays", System-on-Chip, 2008 SOC 2008 International Symposium, pp. 1-4
13. Grigoris Dimitroulakos, Nikos Kostaras, Michalis D. Galanis, Costas E. Goutis: Compiler assisted architectural exploration for coarse grained reconfigurable arrays. ACM Great Lakes Symposium on VLSI 2007, pp. 164-167
14. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis: Improving performance and energy consumption in embedded microprocessor platforms with a flexible custom coprocessor data-path. ACM Great Lakes Symposium on VLSI 2007, pp. 2-7
15. Grigoris Dimitroulakos, Michalis D. Galanis, Nikos Kostaras, Costas E. Goutis: A unified evaluation framework for coarse grained reconfigurable array architectures. Conf. Computing Frontiers 2007, pp. 161-172
16. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis: Speedups and Energy Savings of Microprocessor Platforms with a Coarse-Grained Reconfigurable Data-Path. IPDPS 2007: 1-8
17. Michalis D. Galanis, Grigoris Dimitroulakos, Costas E. Goutis: Performance Optimization of Embedded Applications in a Hybrid Reconfigurable Platform. PATMOS 2007: 352-362
18. G. Dimitroulakos, M.D. Galanis, C.E. Goutis, "Exploring the Design Space of an Optimized Compiler Approach for Mesh-Like Coarse-Grained Reconfigurable Architectures", 20th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2006), pp.10 2006.
19. G. Dimitroulakos, M.D. Galanis, C.E. Goutis, "Resource Constrained Modulo Scheduling for Mesh-Like Coarse-Grained Reconfigurable Architectures", IEEE International Symposium on Circuits & Systems Conference (ISCAS 2006), pp. 2901-2904, 2006.
20. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Mapping DSP Applications on Processor Systems with Coarse-Grain Reconfigurable Hardware", 20th

IEEE International Parallel and Distributed Processing Symposium (IPDPS 2006), Reconfigurable Architectures Workshop (RAW), pp. 8, 2006.
21. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Design Flow for Optimizing Performance in Processors Systems with on-chip Coarse-Grain Reconfigurable Logic", 20th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2006), pp. 10, 2006.
22. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Accelerating DSP Applications in Embedded Systems with a Coprocessor Data-Path", Communication Systems, Networks and Digital Signal Processing (CSNDSP 2006), IEEE Press, pp. 495-499, 2006.
23. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Performance Improvements in Microprocessor Systems Utilizing a Coprocessor Data-Path", International Conference SAMOS (IC-SAMOS), IEEE Press, pp. 85-92, 2006.
24. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Improving Performance of Embedded Processors with a High-Performance Coarse-Grained Reconfigurable Data-Path", 13th IEEE Mediterranean Electrotechnical Conference (MELECON 2006), pp. 105-108, 2006.
25. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Mapping DSP Applications on Processor/Coarse-Grain Reconfigurable Array Architectures", IEEE International Symposium on Circuits & Systems Conference (ISCAS 2006), pp. 3666-3669, 2006.
26. G. Dimitroulakos, M.D. Galanis, C.E. Goutis, "A Compiler Method for Memory-Conscious Mapping of Applications on Coarse-Grained Reconfigurable Architectures", 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2005), Reconfigurable Architectures Workshop (RAW 05), pp. 160b-160b, 2005.
27. G. Dimitroulakos, M.D. Galanis, C.E. Goutis, "Alleviating the Data Memory Bandwidth Bottleneck in Coarse-Grained Reconfigurable Arrays", IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP 2005), IEEE Computer Society Press, pp. 161-168, 2005.
28. G. Dimitroulakos, M.D. Galanis, C.E. Goutis, "Performance Improvements using Coarse-Grain Reconfigurable Logic in Embedded SoCs", Field Programmable Logic and Applications Conference (FPL 2005), IEEE Press, pp. 630-635, 2005.
29. G. Dimitroulakos, M. D. Galanis, A. Milidonis, and C.E. Goutis, "A High-Throughput and Memory Efficient 2-D Discrete Wavelet Transform Hardware Architecture for JPEG2000 Standard", IEEE International Symposium on Circuits & Systems Conference (ISCAS 2005), pp. 4641-4644, 2005.
30. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "An Automated Methodology for Memory-Conscious Mapping of DSP Applications on Coarse-Grain Reconfigurable Arrays", IEEE International Symposium on Circuits & Systems Conference (ISCAS 2005), pp. 3519-3522, 2005.
31. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Accelerating Applications by Mapping Critical Kernels on Coarse-Grain Reconfigurable Hardware in Hybrid Systems", 13th IEEE Field-Programmable Custom Computing

Machines Symposium (FCCM 2005), IEEE Computer Society Press, pp. 300-301, 2005.

32. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Speedups from Partitioning Critical Software Parts to Coarse-Grain Reconfigurable Hardware", IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP 2005), IEEE Computer Society Press, pp. 50-55, 2005.
33. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Partitioning DSP Applications to Different Granularity Reconfigurable Hardware", 12th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2005).
34. M. D. Galanis, G. Dimitroulakos, A. P. Kakarountas, C. E. Goutis, "Speedups from Partitioning Software Kernels to FPGA Hardware in Embedded SoCs", IEEE Workshop on Signal Processing Systems (SIPS 2005), pp. 485-490, 2005.
35. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, "Performance Gains from Partitioning Embedded Applications in Processor-FPGA SoCs",Power and Timing Modelling, Optimization and Simulation Workshop (PATMOS 2005), Lecture Notes in Computer Science (LNCS) 3728, Springer, pp. 247-256, 2005.
36. Milidonis, G. Dimitroulakos, M. D. Galanis, G. Theodoridis, C.E. Goutis, and F.Catthoor, " An Automated C++ Code and Data Partitioning Framework for Data Management of Data-Intensive Applications", 8th International Workshop on Software and Compilers for Embedded Systems (SCOPES 2004), Lecture Notes in Computer Science (LNCS) 3199, Springer, pp. 122-136, 2004.
37. G. Dimitroulakos, A. Milidonis, M. D. Galanis, G. Theodoridis, C.E Goutis and F. Catthoor, "Power Aware Data Type Refinement on the HIPERLAN/2", IEEE International Circuits and Systems Symposium (ICECS 2003), Page(s):216 - 219 Vol.1,2003
38. G. Dimitroulakos, N.D Zervas, N. Sklavos, and C.E. Goutis, "An efficient VLSI implementation for forward and inverse wavelet transform for JPEG2000",IEEE International Digital Signal Processing Symposium (DSP 2002), Page(s):233 - 236 vol.1, 2002

Book Chapters (1)

1. XMSIM : Extensible Memory Simulator for Early Memory Hierarchy Evaluation to appear in the book Designing Very Large Scale Integration Systems: Emerging Trends & Challenges, Lecture Notes in Electrical Engineering LNEE

Awards (2)

1. M. D. Galanis, G. Dimitroulakos, A. P. Kakarountas, C. E. Goutis, "Speedups from Partitioning Software Kernels to FPGA Hardware in Embedded SoCs", IEEE Workshop on Signal Processing Systems (SIPS 2005), pp. 485-490, 2005. (**Best Student Paper**)
2. M. D. Galanis, G. Dimitroulakos, C. E. Goutis, “Improving Performance and Energy Consumption in Embedded Microprocessor Platforms with a Flexible Custom Coprocessor Data-path”, ACM Great Lakes Symposium on VLSI (GLSVLSI 2007), Stresa-Lago Maggiore, Italy, March 11-13, 2007. (**Best Paper Award**)